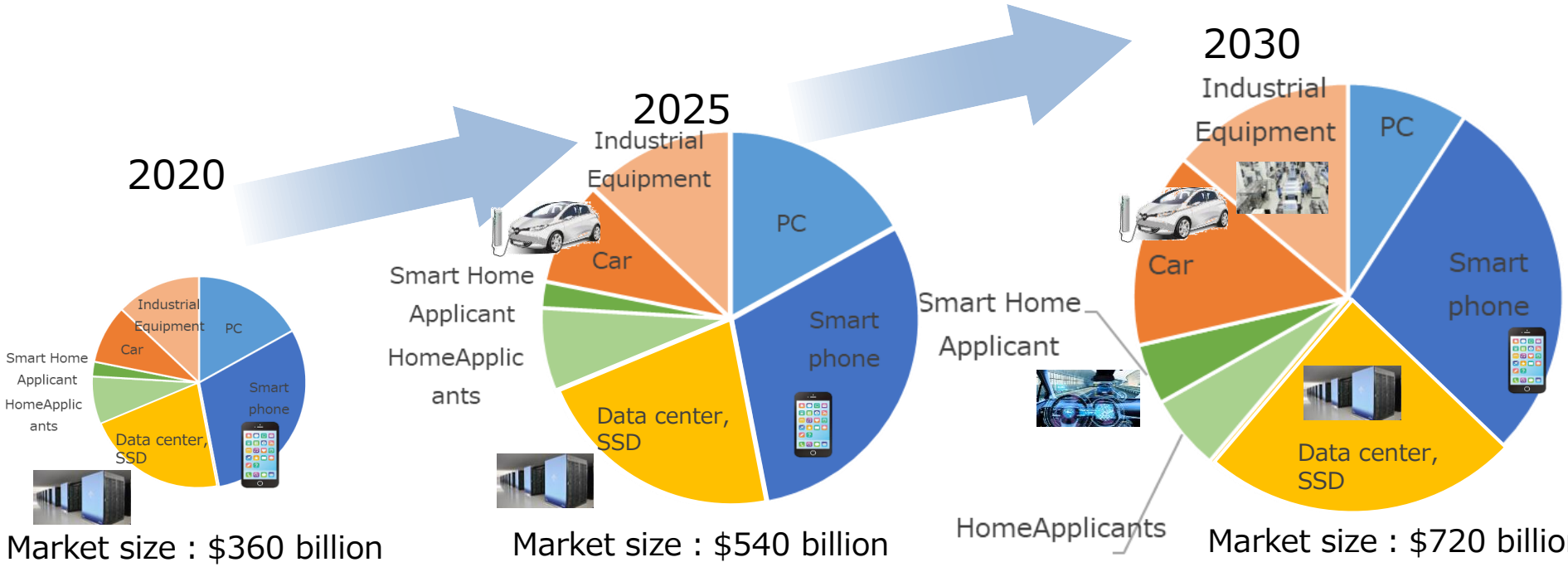
Outline of Semiconductor Revitalization Strategy in Japan

July 2024

Commerce and Information Policy Bureau, Ministry of Economy, Trade and Industry

Basic Semiconductor Revitalization Strategy in Japan

Step 1: Enhancement of Basic Production Capacity for IoT



Step 2: Realization of Next-Gen Semiconductor Technology through US–JP Collaboration

Step 3: R&D For Future technology

Photonics-Electronics Convergence, Quantum Computing through Global Collaboration

Source: prepared by METI based on data from OMDIA

Overview of the Future Semiconductor Strategy I

	Step 1 **Securing manufacturing infrastructures to meet the recent demand**	**Step 2** **Establishing next-generation technologies**	**Step 3** **R&D of future technologies**
Advanced logic semiconductors	✓ Developing domestic manufacturing bases and advancing related technologies	✓ Developing technologies for manufacturing 2 nm-generation logic semiconductors => Realizing mass production ✓ R&D to go beyond-2 nm devices (LSTC)	✓ R&D to go beyond-2 nm devices (LSTC) ✓ Developing future game-changing technologies, e.g., photoelectric fusion
Advanced memory semiconductors	✓ Developing reliable domestic bases for designing and manufacturing through Japan-U.S. collaboration and advancing related technologies	✓ Enhancing the performance of NAND and DRAM ✓ Developing innovative memories	✓ Developing embedded memories
Specialty semiconductors for industrial purposes	✓ Strengthening production infrastructures for power semiconductors through business collaboration and reconstruction in Japan ✓ Building a system for the stable supply of application-based conventional semiconductors that copes with the expansion of industrial demand, e.g., diversified and multifunctional edge devices	✓ Enhancing the performance of SiC power semiconductors and reducing the cost thereof	✓ Developing GaN/Ga2O3 power semiconductors to commercialize them
Advanced packaging	✓ Establishing bases for developing advanced packaging	✓ Establishing chiplet technology	✓ Realizing and implementing optical chiplets and SoC with both digital and analog chips embedded
Manufacturing equipment and parts or raw materials	✓ Building a system for the stable supply of manufacturing equipment and parts or raw materials that are indispensable for manufacturing advanced semiconductors	✓ Developing technologies to commercialize next-generation materials that are necessary for beyond-2 nm devices	✓ Developing technologies to commercialize future materials

Overview of the Future Semiconductor Strategy II

Human resource development	✓Human resource development under regional public-industry-academia collaboration tailored to regional characteristics (e.g., consortiums for human resource development) ✓Developing professionals and global human resources who will play a leading role in designing and manufacturing next-generation semiconductors
International collaboration	✓Utilizing frameworks via Japan-U.S. ties (e.g., joint task forces) based on the Japan-U.S. Basic Principles on Semiconductor Cooperation, enriching such collaboration, starting with the NSTC and LSTC in the U.S., and working on the development of next-generation semiconductors ✓Advancing collaboration with the EU, Belgium, the Netherlands, the UK, the ROK, Taiwan, and other overseas countries and regions in developing use cases and advancing R&D involving next-generation semiconductors in a manner tailored to the needs of partner countries and regions
Greener semiconductors	✓ Coping with PFAS regulations ✓ Achieving higher integration of semiconductors, optimizing architectures, and developing next-generation materials, thereby realizing higher-performance and greener semiconductors

Semiconductor Budget

FY2021: 774 billion yen ($ 5.5 Billion)

- ✓ Capital for advanced semiconductor (5G Promotion Act): 617 billion yen ($4.4B)
- ✓ Capital for general semiconductor : 47 billion yen ($336M)
- ✓ R&D (Post 5G R&D Fund): 110 billion yen ($786M)

FY2022: Total 1.3 trillion yen ($9 billion)

- ✓ Capital for advanced (5G Promotion Act): 450 billion yen ($3.2 B)
- ✓ Capital for general (Economic Security Act): 368.6 billion yen ($2.6 B)
- ✓ R&D (Post 5G R&D Fund): 485 billion yen ($3.5 B)

FY2023: Total 1.85 trillion yen ($13 billion)

- ✓ Capital for advanced (5G Promotion Act): 632 billion yen ($4.5 B)
  - Advanced logic, etc.
- ✓ Capital for general (Economic Security Act): 575.4 billion yen ($4.1B)
  - Power / analog / material, electronic components
- ✓ R&D (Post 5G R&D Fund): 645.6 billion yen ($4.6 B)
  - Rapidus, design, human resource development, etc.

$1 = 140 yen

Step 1: Advanced Semiconductor Production Capacity ① (5G Promotion Act)

Subsidy is based on JPY.
USD is shown only for reference and numerically converted with an example rate of 150 JPY/USD.

1．JASM (Joint Venture of TSMC (TW), Sony (JP) and Denso (JP))
[June 17, 2022]

- ✓Up to **476 billion JPY** (**US$3.17 billion**) subsidy
- ✓New-Fab for Logic Semiconductor (12–28 nm)

2．KIOXIA (JP) and Western Digital (US) [July 26, 2022]

- ✓Up to approx. **92.9 billion JPY** (**US$620 million**) subsidy
- ✓Advanced 3D NAND Flash Memory Investment

3. Micron (US) [September 30, 2022]

- ✓Up to approx. **46.5 billion JPY** (**US$310 million**) subsidy
- ✓Advanced DRAM (1β) Investment

4. Micron (US) [October 3, 2023]

- ✓ Up to **167 million JPY** (**US$1.11 billion**) subsidy
- ✓Advanced DRAM (1γ) Investment including EUV

Step 1: Advanced Semiconductor Production Capacity ② (5G Promotion Act)

Subsidy is based on JPY.
USD is shown only for reference and numerically converted with an example rate of 150 JPY/USD.

5．KIOXIA (JP) and Western Digital (US) [February 6, 2024]

- ✓Up to **150 billion JPY** **(US$1.00 billion)** subsidy
- ✓Advanced 3D NAND Flash Memory Investment

6．JASM (Joint Venture of TSMC (TW), Sony (JP), Denso (JP) and Toyota (JP))

[February 24, 2024]

- ✓Up to **732 billion JPY** **(US$4.88 billion)** subsidy
- ✓Second-Fab for Advanced Logic Semiconductor (6, 12, 40* nm)

* 40nm is not supported

Total amount of subsidy
1,699 (617 + 450 + 632) billion yen
=US$ 12.6 (4.1+3.0＋4.2) billion

Economic Effects of JASM's Investment in Kumamoto

Economic Ripple Effect Estimation (by Kyushu Financial Group)

- ✓ The economic ripple effect over the 10 years from 2022 to 2031 is estimated as **US＄51 billion**. (Including Sony and Mitsubishi Electric investments)
- ✓ **About 90 bases and facilities** are expected to be developed in Kumamoto Prefecture.
- ✓ Creating approximately **10,700 jobs**, including **1,700 jobs** of JASM

Impacts already apparent

- ✓ JASM's monthly salary is **50,000 yen or more higher than the national average.**
- ✓ After the announcement of the JASM's investment, **many firms have announced capital investment plans** throughout Kyushu.

Source: company announcements, media reports, and statistical information

Construction site of TSMC in Kikuyo Town (August 2023)

*Conversion ¥135 per $1

Estimation of Economic Ripple Effect from the Advanced-Semiconductor Fund Project

Analyzed projects

Supplier	Products	Location	Equipment investment	Maximum Subsidy
TSMC/JASM	Advanced logic	Kikuyo Town, Kumamoto Pref.	US＄8.6B scale	476B yen
Kioxia	Memory (NAND)	Yokkaichi City, Mie Pref.	278.8B yen	92.93B yen

Total **568.9B yen**

Economic model	GDP impact (Real)	Employment effect (Total)	Tax revenue effect
CGE model* **Economic ripple effect analysis that is increasingly being adopted internationally** (e.g., the London Olympic games)	About 3.1 trillion yen	About 124K people	About **585.5**B yen

Reference

Direct evaluation model (Evaluation of direct impact)	-	**About 36K people**	**About 600B yen**
Interindustry analysis (Estimate ripple effect based on input-output table)	Economic ripple effect: 9.2 trillion yen	About 463K people	About 760B yen

* CGE model: Advanced model of interindustry analysis. It is close to the real economy, considering changes in the economic structure and supply constraints in the labor market etc., and it enables more conservative and long-term analysis than interindustry analysis.

Source: results of investigation by EY

Profile of Economic Security Promotion Act* (ESPA)

* The Act for the Promotion of Ensuring National Security through Integrated Implementation of Economic Measures

- The first legislation which includes **the concept of economic security**
  A basic act for economic security measures under the one legislative purpose bundling together four policy issues:
  - **1) Ensuring a Stable Supply of Critical Items**
  - **2) Ensuring the Stable Provision of Essential Infrastructure Services**
  - **3) Enhancing Development of Advanced Critical Technologies**
  - **4) Non-Disclosure of Selected Patent Applications**
- Called the **Economic Security Promotion Act** under the presumption that the government of Japan must promptly enact from policy fields ready to be legislated and continue to make revisions while recognizing the remaining policy challenges, including the necessity of improving information security of technologies supported by government funds.

Investment Support by the Gov. of Japan Based on ESPA

Category	Target Products	Companies	Subsidy	Publication Dates
Mature-node chips	Power chips	Toshiba D&S Rohm	$0.96B	7 Dec. 2023
	MCU	Renesas Electronics	$118M	28 April 2023
Equipment	Lithography equipment	CANON	$83M	16 June 2023
Materials	Si wafers	SUMCO	$555M	14 July 2023
	SiC wafers	RESONAC	$76.3M	16 June 2023
	SiC wafers	Sumitomo Electric Industries	$74.1M	16 June 2023
	Package substrates	IBIDEN	$300M	28 April 2023
	Package substrates	Shinko Electric Industries	$132M	16 June 2023
Raw materials	Gas (yellow phosphorus, helium, neon)	Sumitomo Corp. Koatsu Gas Kogyo, KIOXIA, Sony, etc.	$199M	16 June 2023 28 July 2023 6 Dec. 2023

1 $=135 yen

Establishing Tax Concessions for Promoting Domestic Production in Strategic Areas

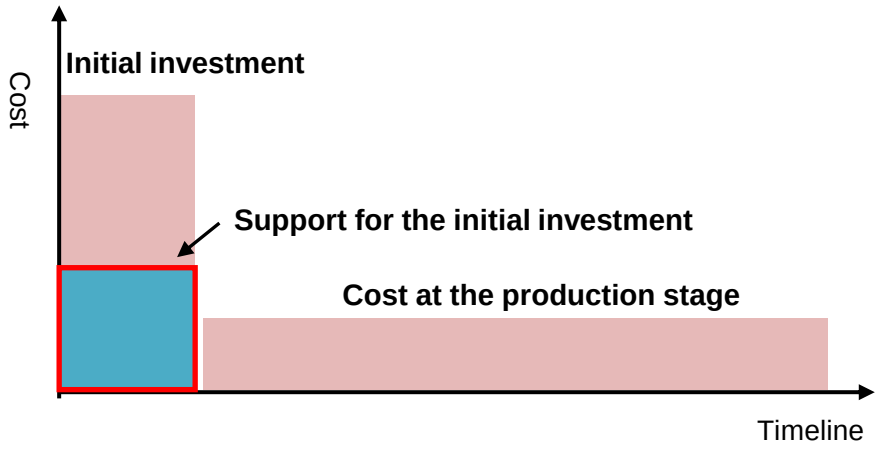
Step 1

(Corporate Tax)

- **A global industrial policy competition is intensifying** to strongly promote domestic investments in strategic areas, as seen in the IRA and CHIPS in the U.S. and the Green Deal Industrial Plan in Europe. Japan as well needs to establish some **investment promotion measures that help it to compete on par with the rest of the world**.
- Specifically, focusing on the strategic areas with **large total business costs, especially business with high costs at the production stage**, including **electric vehicles, green steel, green chemicals, SAF, and semiconductors (e.g., microcomputers and analog semiconductors)**, **Japan as well needs to develop new investment promotion measures that provide tax concessions in accordance with production and sales volumes, taking into account industrial structures**, against the backdrop that investors cannot easily decide on investments in Japan only based on the initial investment promotion measures and that **the U.S. has started support measures provided to companies at the production and sales stages under the IRA**.
- These new investment promotion measures will not only **provide strong incentives to companies to expand production and sales** but also help **accelerate the creation of markets for the highly innovative products** covered by the tax break.

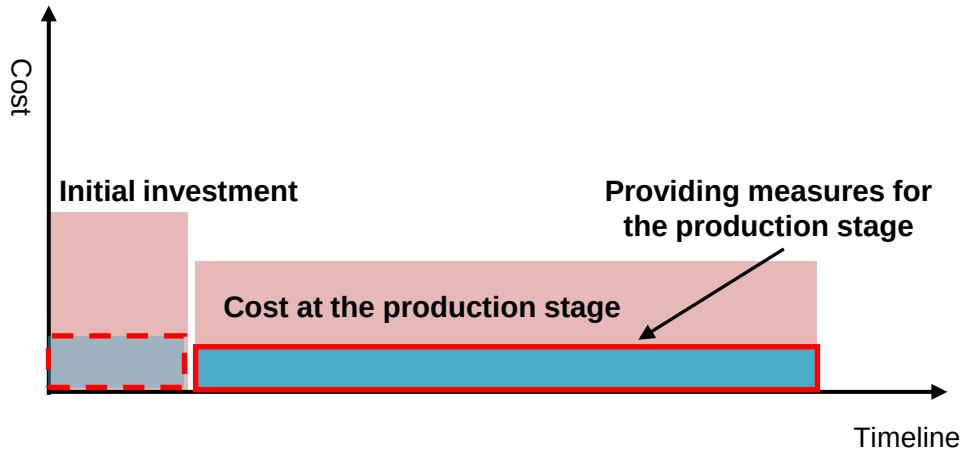
Business with a large proportion of initial investments

⇨ **Support for initial investments is effective.**



Business with a large cost at the production stage

⇨ **Tax concessions for promoting domestic production in strategic areas is provided.**



Step 2: Beyond 2nm Next Generation Semicon Tech

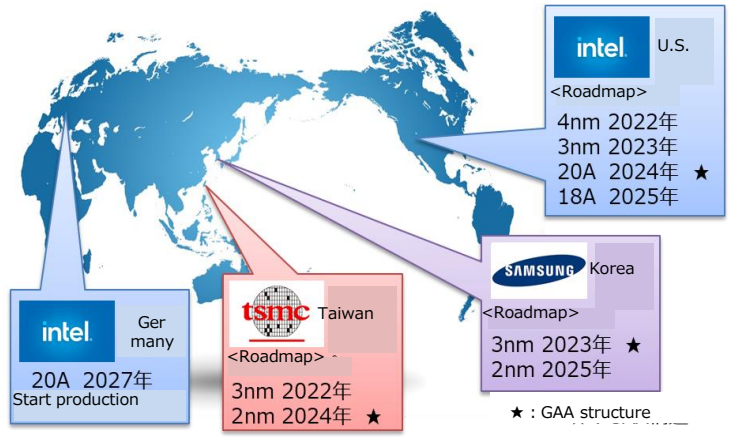
Drastic Technology Change **from Fin-Fet to GAA**

Abroad

Japan

Japan is 10 years behind from Global Trend

Challenges
- ✓ Development of use cases utilizing next-generation semiconductors
- ✓ Establish knowledge of next-generation semiconductor development and manufacturing
- ✓ Education of human resources



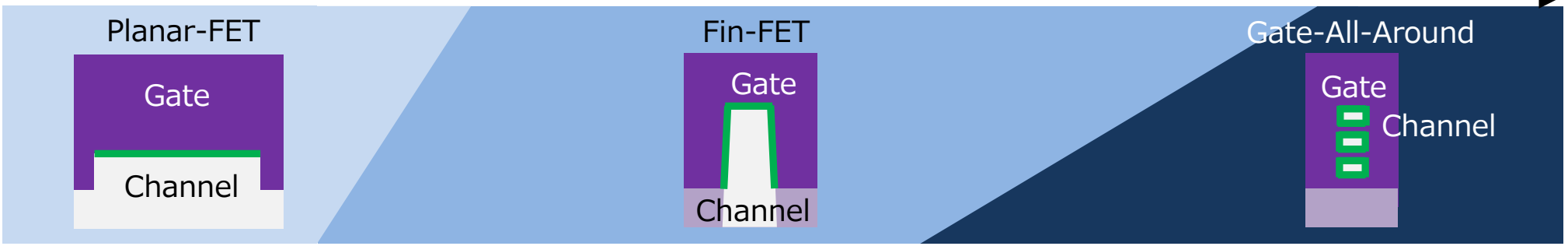
TSMC Japan

Next Generation Semiconductor

Fin-FET introduction

GAA introduction (plan)

45nm 28nm 22nm 16/12nm 7nm 5nm 3nm 2nm Beyond



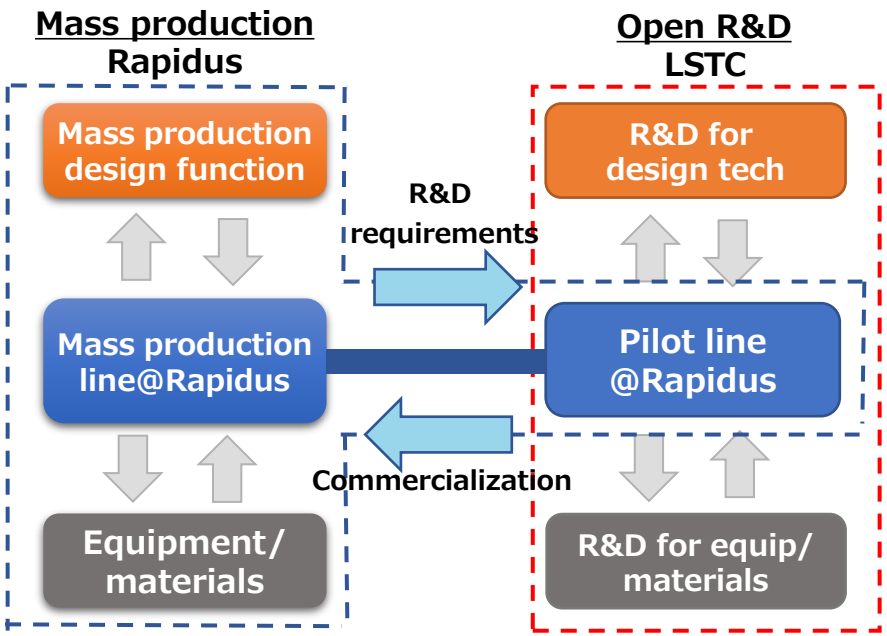
Same gate width in a smaller area ＝high integration

Project Framework for Next Generation Beyond 2nm Project (B2P)

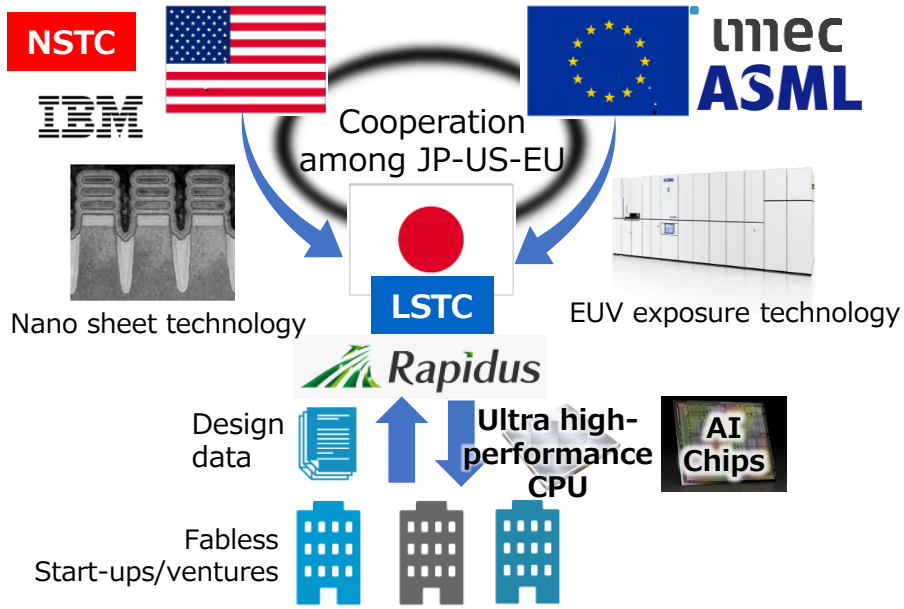
METI announcement on 11 Nov.: Establishment of Two Entities for B2P

1. LSTC:* Open collaborative R&D platform *Leading-Edge Semiconductor Technology Center
2. Rapidus: Mass production entity (Inc.)

Project framework



Cooperations among partner organizations



Use cases

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Progress of Next-Generation Semiconductor R&D Projects by Rapidus

- In November 2022, Rapidus was selected for a next-generation semiconductor R&D project under the Post-5G Fund Project.[1] (Maximum aid in FY2022 and FY2023: 330 billion yen).
  1. Post-5G Information and Communication System Infrastructure Enhancement R&D Project
- Rapidus' **FY2024 plan and budget for this project have been approved** (**maximum aid for FY2023: 536 billion yen**[2]).
- In addition, the project was adopted in March 2024 for **R&D on the enhancement of advanced packaging technology** (**maximum aid for FY2023: 54 billion yen**[2]).

  2. Part of the 677 billion yen allocated in the FY2023 additional budget for the Post-5G Fund Project

Initiatives of Rapidus

FY2022 (Maximum aid: 70B yen)
(467M USD)

Front-end process
(Maximum aid: 70B yen)

- Selected **Chitose City, Hokkaido,** as the planned site for the construction of a manufacturing base
- Joint development partnership with **IBM**
- MOC with **Imec**
- Order **EUV lithography equipment**
- Develop specifications for equipment, conveyance systems, and production management systems required for short TAT production systems

FY2023 (Maximum aid: 260B yen)
(1.7B USD)

Front-end process
(Maximum aid: 260B yen)

- Foundation work for a pilot line in Chitose City, Hokkaido
- **Researchers dispatched** to **IBM Albany Research Center**
- Join **Imec's core programs**
- Development of equipment, transport systems, and production management systems required for short TAT production systems

FY2024 (Maximum aid: 590B yen)
(3.9B USD)

Front-end process
(Maximum aid: 536B yen)

- **Start installation of equipment** on a pilot line in Chitose City, Hokkaido
- **Dispatch of engineers to IBM, upgrade 2nm manufacturing technology**
- Development of equipment, transportation system, and production control system for short TAT

Back-end process
(Maximum aid: 54B yen)

- Start development of **advanced packaging technologies** (Large-scale panels, interposers, 3D packaging technology, etc.)
- International collaboration with IBM, Fraunhofer, and A*STAR

Latter half of 2020s

- Construction of a short TAT pilot line for 2nm generation semiconductors and demonstration using test chips
- Commercialization as an advanced logic foundry based on the results

Rapidus

1 USD=150 yen

LSTC (Leading-edge Semiconductor Technology Center: Japan NSTC)

LSTC was established in 2022 and the leaders of each team were assigned.
R&D items along with needs from industry are under discussion in each team.

Chairman
HIGASHI Tetsuro

Committee for R&D planning
ISHIMARU Kazunari (Rapidus)
MASAHARA Meishoku (AIST)
KURODA Tadahiro (University of Tokyo)
HIRAMOTO Toshiro (University of Tokyo)
SUGAWA Shigetoshi (Tohoku University)
CHIKYO Toyohiro (NIMS)
SUGANUMA Katsuaki (Osaka Univ.)
KOIKE Atsuyoshi (Rapidus)

Chief in Academia
GONOKAMI Makoto

Chip Design
KURODA Tadahiro

Physical Transistor Design
HIRAMOTO Toshiro

Productization Technology
SUGAWA Shigetoshi

Materials Technology
CHIKYO Toyohiro

Advanced Packaging
SUGANUMA Katsuaki

Use-Case Creation
TBD

Human-Resource Development
TBD.

Participating Organizations

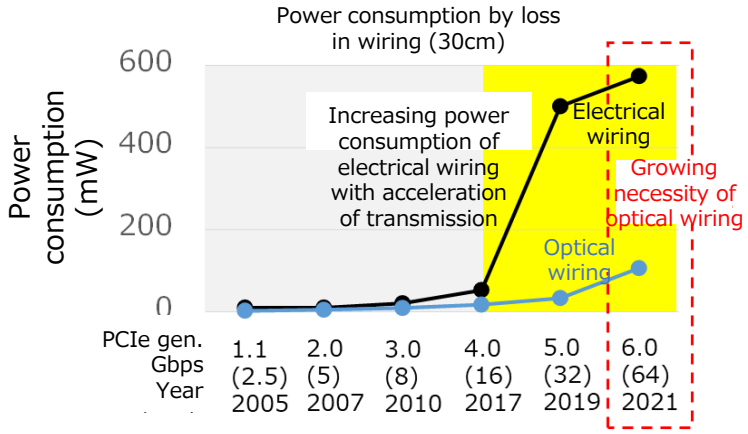
AIST ADVANCED INDUSTRIAL SCIENCE AND TECHNOLOGY (AIST) / RIKEN / NIMS 国立研究開発法人 物質・材料研究機構 National Institute for Materials Science / Rapidus
東京大学 THE UNIVERSITY OF TOKYO / 東北大学 TOHOKU UNIVERSITY / 東京工業大学 Tokyo Institute of Technology / 筑波大学 University of Tsukuba / 大阪大学 OSAKA UNIVERSITY / 名古屋大学 NAGOYA UNIVERSITY / KEK / 北海道大学 HOKKAIDO UNIVERSITY / 広島大学 / 九州大学 KYUSHU UNIVERSITY

Development of Leading-Edge Photonics-Electronics Convergence Technology

Step 3

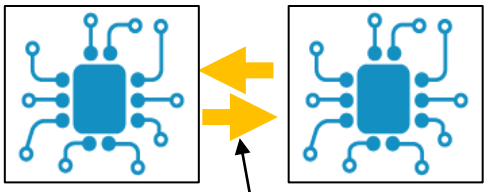
- **To achieve innovative energy conservation in data centers, photonics-electronics convergence technology has emerged as a game-changing technology.**
- **Photonics-electronics convergence technology integrates optoelectronics with electronic devices and replaces electrical wiring with optical wiring, thereby achieving energy saving, increased capacitance, and low latency (1/100 of the power consumption in the entire network system).**
- This project aims to **significantly improve energy efficiency by more than 40% for data centers** that are data aggregation bases by using innovative **photonics-electronics convergence technology,** converting electrical wiring in servers to optical wiring.

■Effect of optical wiring on suppression of power consumption



Power consumption due to electrical wiring is rapidly increasing with the growth of data transmission speed. Use of optical wiring is indispensable for reducing power consumption.

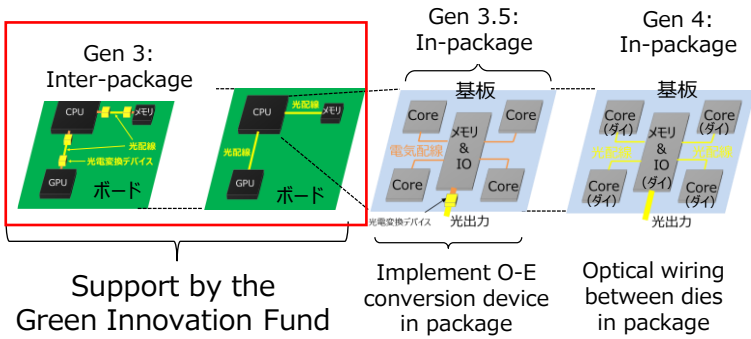
■Photonics-electronics convergence in servers

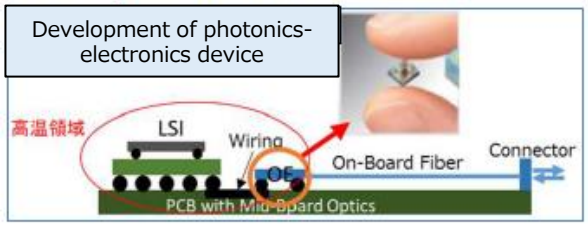


Semiconductor
- CPU
- Accelerator
- Memory

From electrical wiring to optical wiring

■Roadmap for development of photonics-electronics convergence technologies





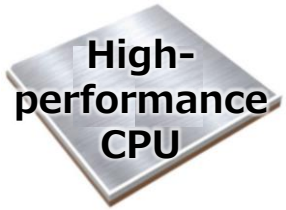
Progress of R&D Project through LSTC

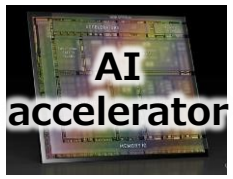
- Public announcement for applications are now being made for **(i) next-generation semiconductor technology development, (ii) photonics-electronics convergence technology development.**
- The evaluation process will be conducted by the end of this year, with the adoption of **the project to be announced at the beginning of the next year**.

(i) Next-generation semiconductor tech.

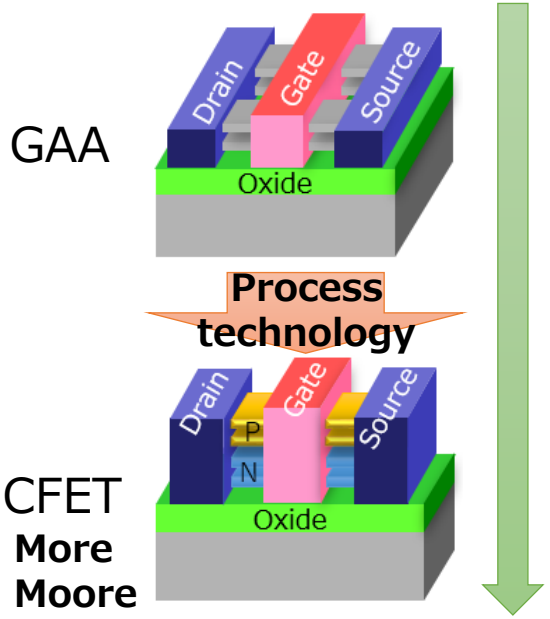
①Chip design by using 2nm-node devices
②Manufacturing technology for Beyond 2nm devices

①Chip design



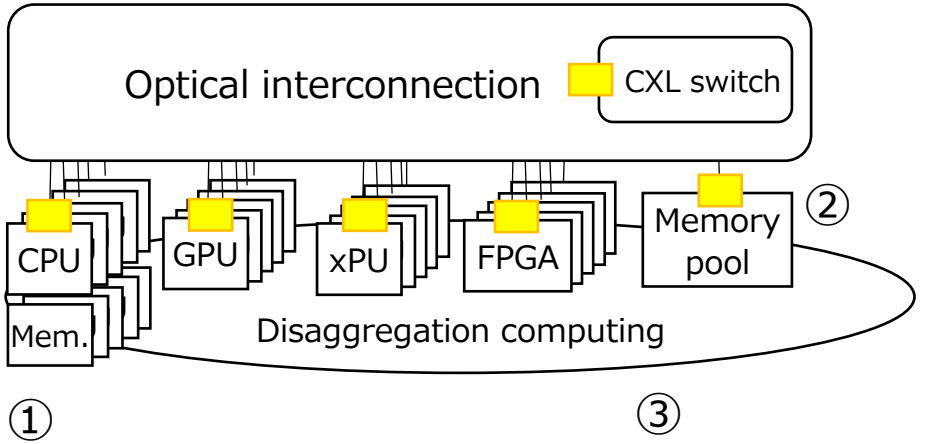


②Beyond 2nm manufacturing technology



(ii) Photonics-electronics convergence tech.

①Optical chiplet packaging technology
②Memory technology with photonics-electronics convergence interface
③Computing technology using photonics-electronics convergence



Design of AI Chips

- The use of AI requires a large amount of computation. Reducing power consumption may become an issue.
- Efforts are underway to improve power efficiency in processing by using semiconductors specialized for each application. Utilization of dedicated semiconductors through co-design of software and hardware is essential.
- Dedicated semiconductors defined from system and software requirements for specific applications such as automobiles and communications will be developed for significant reduction of power consumption.

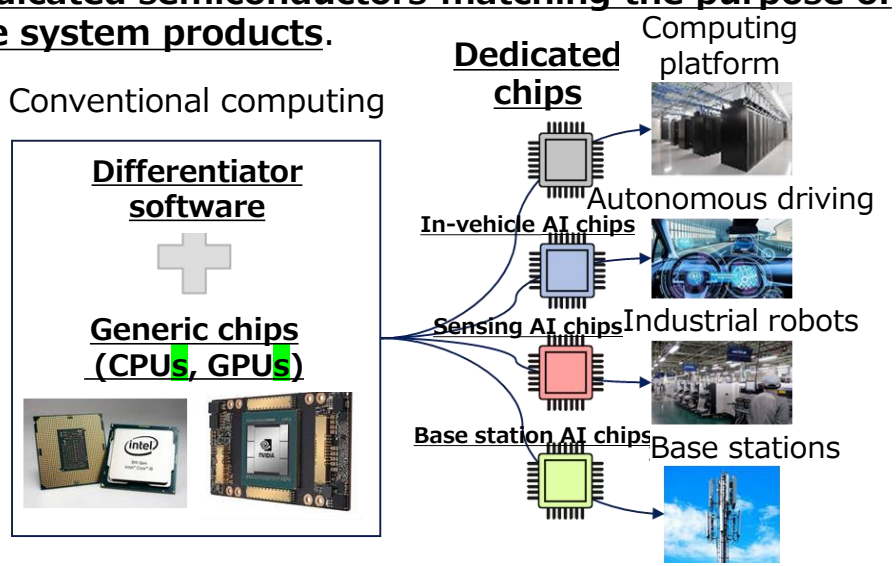
Examples of dedicated semiconductors

Tesla designs its own semiconductors for autonomous driving. Cloud platformers such as GAFAM are not only using but also designing dedicated semiconductors.

Company	Application	Node
TESLA	Autonomous driving	14nm
	Super computers	7nm
Apple	Smartphones	5nm
	Desktops	5nm
Google	AI chips	7nm
aws	Servers	5nm
	AI chips	N/A
Microsoft / GRAPHCORE	AI chips	7nm
Meta	AI chips	N/A

SoC (System-on-Chip) development

SoCs are tech-intensive semiconductors combining major computing components such as microprocessors, chipsets, video chips and memories. They enable **dedicated semiconductors matching the purpose of the system products**.



Status of Initiatives for Development of Semiconductor-related Human Resources

- For developing/securing human resources supporting the semiconductors industry, in addition to individual activities involving industry/academia/government, **regional initiatives through those collaborations** are necessary. Six regions have already started the initiatives.
- **Development of global professional human resources** for semiconductor design and manufacturing is pursued mainly through LSTC for establishment of a design/manufacturing platform for next-gen semiconductors in Japan.

Regional initiatives

Note: Initiatives by industry-academia-government collaboration are started in six regions by June 2023.

Kyushu Semiconductor Human Resources Development Consortium

(Industry) Sony, JASM, etc.
(Academia) Kyushu Univ, etc.
(Government) Kyushu Bureau of METI, Kumamoto Pref., etc.

✓ Considering creation of content for dissemination, etc.

Tohoku Semiconductor and Electronics Design Study Group

(Industry) KIOXIA Iwate, etc.
(Academia) Tohoku Univ., etc.
(Government) Tohoku Bureau of METI, Iwate Pref., etc.

✓ Considering company visits, creation of PR videos, etc.

Chugoku Region Semiconductor Industry Promotion Council

(Industry) Micron, etc.
(Academia) Hiroshima Univ, etc.
(Government) Chugoku Bureau of METI, Hiroshima Pref., etc.

✓ Considering creation of skill maps, holding workshops, etc.

Chubu Semiconductor Human Resource Development Council

(Industry) KIOXIA, etc.
(Academia) Nagoya Univ., etc.
(Government) Chubu Bureau of METI, Mie Pref., etc.

✓ Considering fab tours, internships and special lectures, etc.

Hokkaido Semiconductor Human Resources Development Promotion Council

(Industry) Rapidus, etc.
(Academia) Hokkaido Univ, etc.
(Government) Hokkaido Bureau of METI, Hokkaido, etc.

✓ Considering creation of roadmaps, etc.

Kanto Semiconductor Human Resource Development Council

(Industry) Renesas, etc.
(Academia) Ibaraki Univ., etc.
(Government) Kanto Bureau of METI, Ibaraki Pref., etc.

✓ Considering holding PR events, visualizing HR development needs, etc.

Industry initiatives

✓ On-site classes, fab tours, contributions to curriculums formation by JEITA, etc.

Academia initiatives

✓ HR development through curriculums in colleges and R&D in universities, etc.

Government initiatives

✓ Holding digital human resource development council meetings, etc.

LSTC initiatives

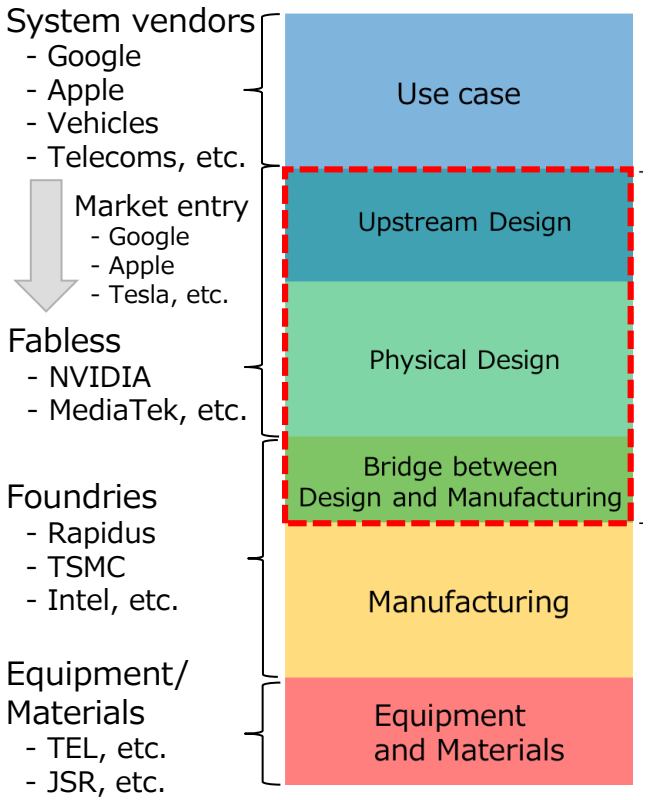
Plus

✓ Aim for development of global professional human resources to establish a next-gen chip design and manufacturing platform in the late 2020s.

Development of Skilled Human Resource

- Regional consortiums have been established basically for operation of production lines.
- Concrete projects will be formed for **development of skilled human resources capable of creating new businesses utilizing next-gen semiconductors**.
- Design of semiconductors is the most prioritized area in skilled HR development. **A three-tier curriculum is being discussed with worldwide industries/academia**.

Trends of design



Goal

Producing human resources well-versed in HW/SW as well as architecture

Advanced

Practical curriculum of HW/SW/Architecture necessary for design of CPU/GPU in collaboration with global top companies

Intermediate

Design curriculum for 12-28nm chips (volume zone in Japan)

Elementary

Basic programs such as how-to on EDA tools

Recent Updates on International Cooperation

[JP-US] Basic Principles on Semiconductor Cooperation (May 4, 2022)	✓ **Both cooperate in the semiconductor supply chain bilaterally in accordance with the following basic principles:** 1. Based on open markets, transparency, and free trade 2. With a shared objective to **strengthen supply chain resiliency in Japan, the United States, and other like-minded countries and regions** 3. In a mutually accepted and complementary manner
[JP-US] Joint Statement for the 2nd ministerial meeting of the JUCIP (May 26, 2023)	✓ Under the Japan-U.S. Joint Task Force established based on the Basic Principles for Semiconductor Cooperation, both agreed to **promote collaboration in the field of next-generation semiconductors** and to **promote cooperation between the U.S. NSTC, which is scheduled to be established in the future, and the LSTC in Japan**.
[JP-EU] MOC on Semiconductors (Jul 4, 2023)	✓ Both agreed on cooperation for the **Early Warning Mechanism for the semiconductor supply chain**, **R&D for next-gen semiconductor technologies**, **development of advanced skills**, **use cases of cutting-edge semiconductor applications**, etc. ➔ **Japan-EU Semiconductor Workshop on Jan. 25**
[JP-UK] Semiconductor Partnership (May 18, 2023)	✓ METI and DSIT will engage in **joint research and development in fields with mutual strengths, such as cutting-edge semiconductor design, manufacturing, and advanced packaging etc.**, conduct **public-private dialogue** on the UK-Japan semiconductor industry, and dispatch **expert missions**. ➔ **Japan-UK Semiconductor Workshop on March 27**
[JP-NL] MOC on Semiconductor Cooperation (June 21, 2023)	✓ Both promote **cooperation among governments, industries and institutes in the areas of semiconductors and photonics, etc.**, and **cooperation between the LSTC in Japan and the Competence Centre in the Netherlands**, while commonly recognizing the significant importance of the R&D project of Rapidus Corp. ➔ **Semiconductor Mission from Japan to the Netherlands in March**
[JP-IN] MOC on semiconductor Partnership (July 20, 2023)	✓ Establish the Japan-India Semiconductor Supply Chain Policy Dialogue and (1) **consider initiatives to enhance semiconductor supply resilience** based on mutual strengths, (2) **promote talent and workforce development**, (3) **explore areas of mutually beneficial R&D collaboration**, and (4) **promote intellectual property protection**, etc.
[JP-IT] Joint Statement (Dec 12, 2023)	✓ **Explore the possibility of cooperation including joint industrial research projects in sectors of mutual interest and priority, such as semiconductors**, biotech, energy, mobility and others