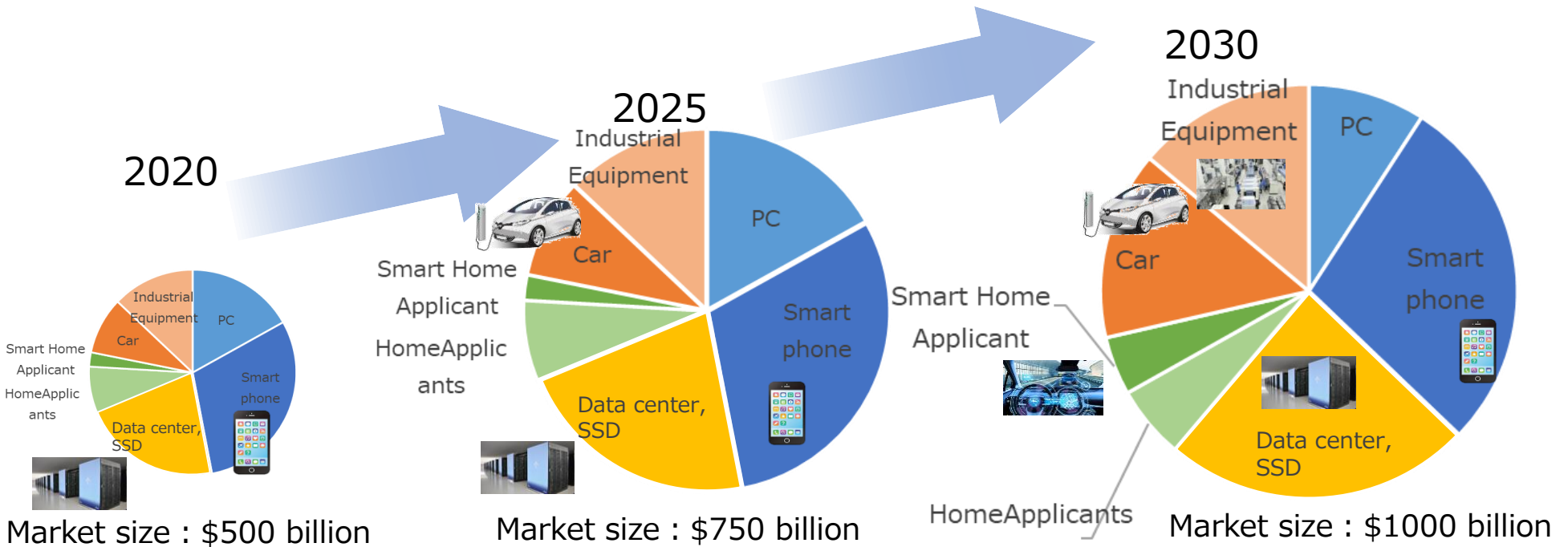


Basic Semiconductor Revitalization Strategy in Japan

Step 1 : Enhancement of Basic Production Capacity for IoT



Step 2 : Realization of Next Generation Semiconductor Technology through JP-US Collaboration

Step 3 : RD For Future technology Photonics-Electronics Convergence, Quantum Computing through Global Collaboration

(Reference) : prepared by METI, based on data from OMDIA

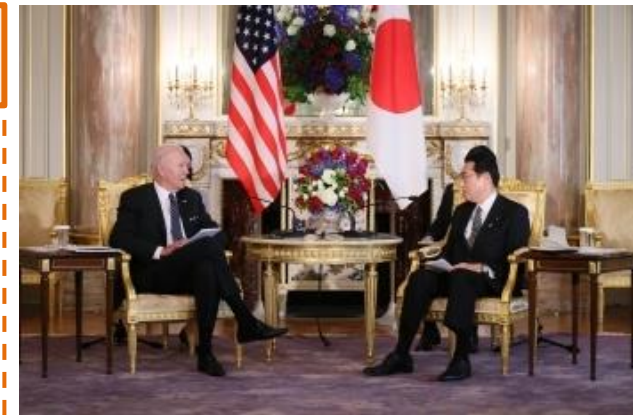
Semiconductor Industry Policy through Japan-US Cooperation

- For the research and development of semiconductors and the resilience of their supply chains, it is essential that allies and like-minded countries and regions work together. Japan and the US are making progress in cooperation on semiconductors at the summit and ministerial levels.
 - On May 4, Mr. HAGIUDA Koichi, then Minister of Economy, Trade and Industry, and Ms. Gina RAIMONDO, US Secretary of Commerce, agreed on the Basic Principles on Semiconductor Cooperation.
 - At the Japan-US Summit Meeting held on May 23, the establishment of a joint task force for developing next-generation semiconductors based on the Basic Principles on Semiconductor Cooperation was announced.
 - At the Japan-US Economic Policy Consultative Committee (Economic 2+2) held on July 29, the two countries agreed to promote joint research and development between them with a view toward fostering and protecting important and emerging technologies. The establishment of a research and development organization (Japan's NSTC) was announced as an initiative on the Japanese side.

Basic Principles on Semiconductor Cooperation (Outline)

(May 4, 2022: Agreement reached between former Minister Hagiuda and US Secretary of Commerce Raimondo)

- The two countries intend that bilateral semiconductor supply chain cooperation be guided by the following basic principles:
 1. Based on open markets, transparency and free trade,
 2. with a shared objective to strengthen supply chain resiliency in Japan, the United States, and other like-minded countries and regions; and
 3. in a mutually accepted and complementary manner
- The two countries will cooperate particularly in the areas of strengthening semiconductor production capacity, promoting workforce development, increasing transparency, coordinating emergency responses to semiconductor shortages, and enhancing R&D cooperation.



May 23 Japan-US
Summit Meeting

[Reference] Basic Policy (Basic Policy on Economic and Fiscal Management and Reform 2022)

○ Chapter 3: Responding to changes in the internal and external environments

1. Responding to changes in the international environment

(2) Strengthening economic security

(...)

The government will enhance our advanced semiconductor production base and develop human resources in accordance with agreements reached at Japan-US summit meeting, and the government will establish designs and manufacturing production base production base for next-generation semiconductors in the latter half of the 2020s.

October 3, 2022

[Reference] Prime Minister Kishida's general policy speech at the 210th session of the Diet

[Investment and reform for growth]

Next is investment and reform for growth. (...)

The fourth is investment into digital transformation (DX). (...)

In particular, we will put effort into the area of semiconductors, which are indispensable for industries, expected to significantly affect the economy and create jobs, and necessary for economic security. TSMC's base in Kumamoto is predicted to bring over 4 trillion yen to the local economy over ten years and create jobs for more than 7,000 people. Japan is gathering investments in the public and private sectors for the semiconductor field, which is said to require over 10 trillion yen over ten years.

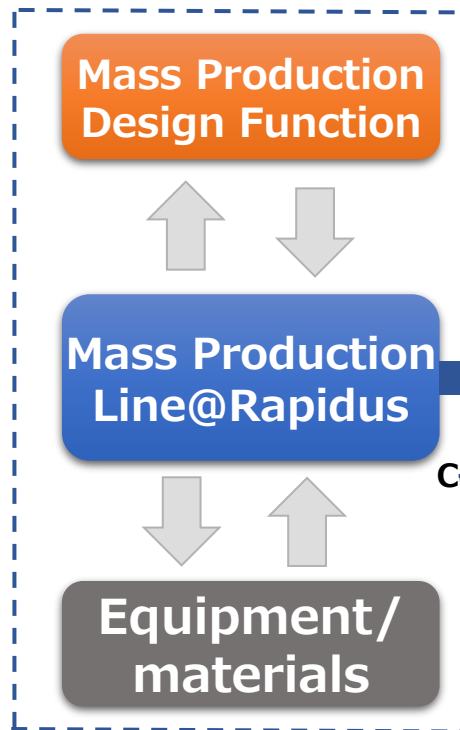
The most recent comprehensive economic stimulus packages will further strengthen the development of leading-edge technologies, including Japan-US joint technological development and mass production of next-generation semiconductors, which are the focus of the packages, and R&D for Beyond 5G. (...)

Project Framework for Next Generation Beyond 2nm Project (B2P)

<METI announcement on 11th Nov.>: Establishment of Two Entities for B2P

1. "LSTC": Open Collaborative R&D Platform (Public Entity) ※Leading-Edge Technology Center
2. "Rapidus": Mass Production Entity (Inc.)

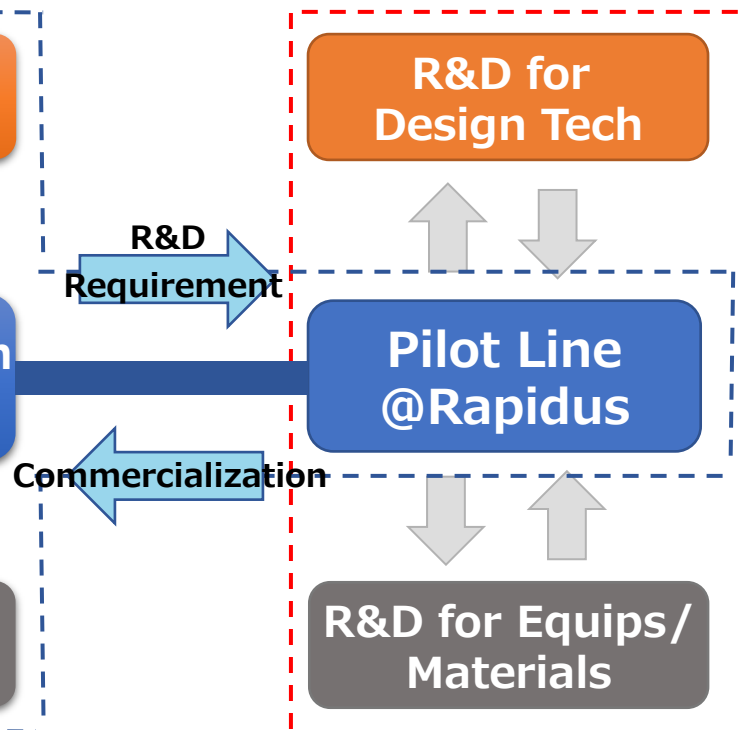
Mass Production "Rapidus"



JP Private Companies

Kioxia, Sony, SoftBank, Denso,
Toyota, NEC, NTT, MUFG

Open R&D "LSTC"



JP Academia

JP National Research Lab

■ Overseas Collaboration

- Research Labs & Academia in Like-minded Countries : US NSTC, IBM, IMEC, etc

■ Domestic Collaboration

- Semicon User Companies
- Digital Design Labs
- Material & Machinery Companies

etc

Research and development base Leading-edge Semiconductor Technology Center (LSTC)

- **The Leading-edge Semiconductor Technology Center (LSTC) will be established this year as a research and development base for developing next-generation-semiconductor mass production technology.**
- LSTC will cooperate with related organizations from overseas including the US NSTC*¹ and build **an open R&D platform for Japan and overseas.** It will form and implement technological development projects related to short TAT*² and 2nm or shorter node technologies to enable the mass production of next-generation semiconductors.
- National research institutes, academia, and industries will come together with the goal of strengthening the competitiveness of Japan's semiconductor-related industries.

*1: National Semiconductor Technology Center, scheduled to be established under the US CHIPS and Science Act

*2: TAT: Turnaround Time

<Key members of the LSTC>

- Chairman: HIGASHI Tetsuro
- Chief in Academia: GONOKAMI Makoto

Name	Position	Overview
KURODA Tadahiro	Committee member responsible for R&D formulation Head of Design Technology Development Division	Establishment of leading-edge semiconductor circuit design technology
HIRAMOTO Toshiro	Committee member responsible for R&D formulation Head of Device Technology Development Division	Development of leading-edge technology for GAA transistors and later
SUGAWA Shigetoshi	Committee member responsible for R&D formulation Head of Process and Equipment Technology Development Division	Development mass production technology for enabling short TAT
CHIKYO Toyohiro	Committee member responsible for R&D formulation Head of Material Development Division	Development of materials for GAA construction and advanced packaging
SUGANUMA Katsuaki	Committee member responsible for R&D formulation Head of 3D Packaging Technology Development Division	Establishment of 3D packaging technology
MASAHARA Meishoku	Committee member responsible for R&D formulation	
KOIKE Atsuyoshi	Committee member responsible for R&D formulation	

Note: Human resource development is also under consideration. In addition, the system may be expanded according to the LSTC's activities.

Note: Committee responsible for R&D formulation: Members who formulate R&D policies and content in the LSTC.

<Participating organizations> National Institute for Materials Science (NIMS), RIKEN, National Institute of Advanced Industrial Science and Technology (AIST), Tohoku University, University of Tsukuba, University of Tokyo, Tokyo Institute of Technology, High Energy Accelerator Research Organization, Rapidus Corporation

Mass production base: Rapidus Corporation

- A company established with the endorsement of major Japanese companies that gathers top-level engineers from all over Japan in order to create a mass production base for next-generation semiconductors.
- It has been selected to carry out the research and development project toward the establishment of design and manufacturing bases for next-generation semiconductors in the latter half of the 2020s.
- Together with LSTC, Rapidus will aim to build a mass production base for next-generation semiconductors in Japan.

■ Rapidus Corporation principal officers and employees

Position	Name
Executive Chairman	HIGASHI Tetsuro
President and Representative Director	KOIKE Atsuyoshi
Corporate Auditor	YAMATO Yasuhiko
Employees	KURODA Rihito* KOBAYASHI Masaharu* TOMIDA Kazuyuki IKEDA Shuji KOYAMA Akio ORII Yasumitsu ENOMOTO Takao NAGAE Shunichiro TANIGAWA Tomokazu

■ Rapidus Corporation outside directors

Position	Name
Outside Director (planned)	KOBAYASHI Yoshimitsu
Outside Director (planned)	NISHI Yoshio
Outside Director (planned)	KOSHIBA Mitsunobu
Outside Director	MATSUO Makoto

The system may be expanded in the future in accordance with Rapidus Corporation's activities.

Note: Concurrent with another post

How the next-generation semiconductor research and development project will proceed

- Rapidus Corporation was selected to carry out the next-generation semiconductor research and development project (development funds: 70 billion yen) under the Post 5G Fund project* (announced on November 11).
- Rapidus Corporation will use the funds to develop the following technologies.
Development theme: Research and development of integration technology for 2 nm-node semiconductors and short TAT production technology based on cooperation between Japan and the US
 - The company will cooperate with IBM and other companies to develop technology for 2 nm-node logic semiconductors, build short TAT pilot lines in Japan, and conduct verifications using test chips.
 - In FY2022, will acquire the elemental technologies for 2 nm-node semiconductors, begin installing EUV lithography equipment, formulate specifications for the equipment, transport systems, and production management systems necessary for the short TAT production system, and deploy the initial design for the pilot line (development costs: 70 billion yen*).
 - Will aim to commercialize the advanced logic foundry after the research period based the results.

Note: Project for Research and Development of Enhanced Infrastructures for Post-5G Information Communication Systems.
70 billion yen of the 110 billion yen in the last fiscal year's supplementary budget will be allocated to this project.

Schedule for the next-generation semiconductor research and development project

- **METI and the US Department of Commerce will continue to manage the progress** of the next-generation semiconductor research and development project through the **Japan-US joint task force** based on the Japan-US Summit agreement.
- **After they are established, the US NSTC and Japan's NSTC (LSTC) will cooperate to gather the best and brightest from both countries.**
- **Japan, the US, and the public and private sectors will divide roles appropriately and cooperate closely** to progress from the R&D stage all the way to commercialization.

